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Citation: Applied Physics Letters **104**, 223112 (2014); doi: 10.1063/1.4881977
View online: http://dx.doi.org/10.1063/1.4881977
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APPLIED PHYSICS LETTERS **104**, 223112 (2014)

Fabrication of sub-12 nm thick silicon nanowires by processing scanning probe lithography masks

Yu Kyoung Ryu,[1] Pablo Aitor Postigo,[2] Fernando Garcia,[2] and Ricardo Garcia[1,a)]
[1]*Instituto de Ciencia de Materiales de Madrid, CSIC, Sor Juana Inés de la Cruz 3, 28049 Madrid, Spain*
[2]*Instituto de Microelectrónica de Madrid (IMM-CNM-CSIC), 28760 Tres Cantos, Madrid, Spain*

(Received 4 May 2014; accepted 26 May 2014; published online 6 June 2014)

Silicon nanowires are key elements to fabricate very sensitive mechanical and electronic devices. We provide a method to fabricate sub-12 nm silicon nanowires in thickness by combining oxidation scanning probe lithography and anisotropic dry etching. Extremely thin oxide masks (0.3–1.1 nm) are transferred into nanowires of 2–12 nm in thickness. The width ratio between the mask and the silicon nanowire is close to one which implies that the nanowire width is controlled by the feature size of the nanolithography. This method enables the fabrication of very small single silicon nanowires with cross-sections below 100 nm^2. Those values are the smallest obtained with a top-down lithography method. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4881977]

Silicon nanowires (SiNWs) are the key elements to design and fabricate highly sensitive devices such as label-free biosensors,[1–3] mass sensors,[4,5] electromechanical resonators,[6,7] or photovoltaic devices.[8] Bottom-up[9,10] and top-down[11–15] approaches aim to produce silicon nanowires with high surface-to-volume ratio and large integration. In particular, top-down lithographies have demonstrated their ability to produce silicon nanowire-based field effect transistors (FETs) with very small sizes and good electrical properties. The high spatial resolution and positioning capabilities of scanning probe lithography[16–19] (SPL) have been exploited to fabricate straight or curved SiNW FETs,[20] and their electrical properties have been characterized.[21] Thermal SPL has created parallel arrays of silicon nanowires with a 55 nm periodicity by combining plasma etching and the use of 4 nm silicon oxide masks.[22]

The optimization of the SiNW devices requires to decrease the size of the devices both in width and height. The fabrication of SiNW FETs by oxidation SPL (o-SPL) relies on the transfer of an oxide pattern (mask) into the active layer of a silicon on insulator (SOI) substrate by etching techniques. Plasma etching, in particular reactive ion etching (RIE),[20,23–25] is preferred over wet etching due to its control over directionality. Those devices have been previously fabricated by using relatively thick silicon-on-insulator samples with an active layer of 55 nm in thickness.[15] The thickness of the active Si layer already imposes some limits in the minimum height of the resulting SiNW. One way to address this issue is by using ultra thin SOI of 12 nm in thickness. However, this requires both the fabrication of oxide masks that are extremely thin ($\sim$1 nm) and having a highly selective etching process. The first requirement is needed to generate small nanowires in width and the latter to remove the unmasked silicon before the mask is consumed. The oxide masks defined by o-SPL are sloped and erode during the etching, consequently the parameters of reactive ion etching, such as radio frequency power, chamber pressure, gas composition, gas flow, or wafer temperature have to be tuned to promote a chemical and anisotropic etching process instead of a sputtering and isotropic etching process.

We report a method to fabricate sub-12 nm thick silicon nanowires by using sub-1.1 nm thick silicon oxide masks. The method combines oxidation scanning probe lithography and anisotropic plasma etching. The probe lithography is used to fabricate extremely thin silicon oxide masks. The plasma etching is controlled by acting on the proportion of oxygen and the chamber pressure. The use of extremely thin masks requires the addition of a certain amount of oxygen to the etching gas (SF_6) to passivate the exposed SiNW sidewalls and to enhance the selective etching of Si versus the mask by favoring chemical processes versus sputtering removal. The fabricated silicon nanowire has a width that coincides with that of the oxide mask. This method enables the fabrication of silicon nanowires with cross-sections below 100 nm^2. Those channel sections are the smallest obtained with a top-down lithography method.

The silicon oxide masks and the transferred silicon nanowires were made on substrates from the same ultra-thin silicon on insulator wafer (MEMC/SunEdison, US). The top (100)-oriented Si layer is 12 nm thick, p-doped, and has a nominal resistivity of 9–15 Ω cm. The buried oxide layer (BOX) has 25 nm of thickness. Markers made of metal pads are defined on the SOI substrate by photolithography and metal evaporation. They are placed to locate the different patterns during the fabrication and characterization steps. Then, the substrate undergoes a cleaning protocol that involves three sonication cycles of 12 min each in a mixture of NH_4OH:H_2O_2:H_2O (1:1:2). Then, the samples are sonicated for 5 min in deionized water.

The atomic force microscope (AFM) and the sample are kept in a closed chamber to control the relative humidity and the temperature during the oxidation process. The o-SPL is performed by operating the AFM in the amplitude modulation mode[26] with a free amplitude in 5–10 nm range and a set point amplitude/free amplitude ratio of about 0.9. We have used n+-doped silicon cantilevers (NCH-W, NanoWorld) with a force constant of about 40 N/m and a resonant frequency about 300 kHz. The relative humidity is kept in 40%–60% range. Voltage pulses of 15–30 V and 0.5 ms were used. The height and width of the silicon nanowires are characterized by taking AFM images of the patterned structures (cross-sections). The

a)E-mail: r.garcia@csic.es.

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silicon oxide mask thickness and width are, respectively, about 0.3–2.5 nm and 20–60 nm. In the text, the width is given as the full width at half maximum (FWHM). Throughout the text, thickness is used to refer size in the vertical direction.

The etching experiments are performed in a reactive ion etching system (PlasmaLab 80, Oxford Instruments, UK). The RIE process for each patterned substrate involves several preliminary steps. Once the sample is introduced in the chamber, the pressure is lowered to 10^{-8} Torr for 1 h. Then there is a purge with N_2 for 1 min. This step is followed by another vacuum cycle at 10^{-8} Torr for 5 min. Then the SF_6:O_2 gas mixture is introduced and let to stabilize for 1 min at the specific chamber pressure of the experiment. In the text, the gas flow is given in units of sccm.

The present method is based on the ability of o-SPL to fabricate and control the thickness of extremely thin oxide masks with a precision of a few tenths of nm. This control is achieved by controlling the voltage between the tip and the sample during the local anodic oxidation process. Additionally, the selectivity between the oxide and the silicon is achieved by promoting chemical etching over sputtering. This is achieved by minimizing the ion current density while having a relatively high concentration of F and some O. The presence of F favors the chemical etching of the silicon while the presence of O helps to passivate the emerging silicon sidewalls slowing down the etching there.

Schemes of the cross-section of some of the patterned silicon oxide masks and the resulting Si nanowires after an etching process are shown, respectively, in Figs. 1(a) and 1(b).

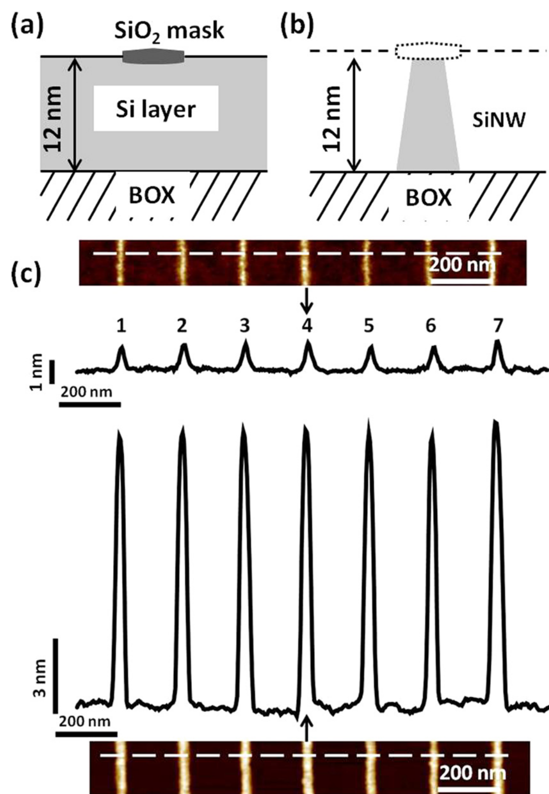

FIG. 1. (a) Scheme of the o-SPL mask and the Si layer of the SOI. (b) Scheme of the SiNW after etching. (c) AFM topographic images and cross sections of an array of oxide masks and their corresponding silicon nanowires after etching. Note that the widths at the bottom of the oxide masks and the SiNWs are very similar.

TABLE I. Heights and widths (FWHM) of the silicon dioxide masks and silicon nanowires labeled 1–7 in Figure 1. The oxide height is measured from the Si baseline.

	H (nm)		W (nm)	
N⁻	SiO_2 mask	SiNW	SiO_2 mask	SiNW
1	1.1	12.7	24	27
2	1.1	13.0	24	34
3	1.3	13.0	34	35
4	1.4	13.1	33	30
5	1.2	12.9	35	33
6	1.1	12.7	29	24
7	1.4	13.5	25	39

Figure 1(c) shows the AFM topographic images and cross-sections of an array of silicon oxide masks and the corresponding silicon nanowires after the etching. The widths and heights of the oxide masks and SiNWs of the above structures are compiled in Table I. The width ratio SiNW:oxide mask is close to 1 while the height ratio is close to 11. The above results have been obtained by using a chamber pressure of 90 mTorr, a gas mixture of SF_6:O_2 in the proportion of (12:3), etching times of 126 s and 10 W of radio frequency power.

Figure 2(a) shows the thickness of the resulting SiNW as a function of the chamber pressure for an O_2 flow of 3 sccm. In this experiment, the radio frequency (rf)-power, the gas ratio, and the etching time are kept fixed at values of 10 W, SF_6:O_2 (12:3), and 126 s. Only under the maximum pressure allowed by the RIE instrument (90 mTorr) used here, the original thickness of the active Si layer is conserved in the etching process. For lower pressures, the thickness of the SiNW decreases monotonically with the decreasing pressure because the o-SPL masks are consumed during the etching cycle (126 s). In the pressure range of 0–100 mTorr, the lower the pressure the higher the ion flux and the lower the concentration of F. This implies that sputtering dominates over the chemical etching. This mechanism reduces the etching selectivity.[27]

The proportion of oxygen to find the optimum selectivity between the oxide and the silicon is found by varying the oxygen flow at a fixed SF_6 flow. Figure 2(b) shows the evolution of the SiNW thickness as function of the O_2 flow. Here, the values of the chamber pressure, SF_6 flow, rf-power, and etching time were, respectively, 90 mTorr, 12 sccm, 10 W, and 126 s. The data show a maximum at 3 sccm, which implies that the original Si layer under the o-SPL mask is preserved during the etching. At lower oxygen flows, the Si layer under the mask is overetched (Fig. 2(c)) (the initial thickness is not conserved). On the other hand, at higher flows the silicon structure is not separated from the rest of the Si layer (underetched) (Fig. 2(d)). The observation of a maximum in the etching rate as the oxygen is increased has been reported for the etching of other structures and materials.[28–31] Each data point shown in Figs. 2 and 3 represents an average taken over 5–10 different masks (or SiNW structures) fabricated under similar identical o-SPL conditions.

The SF_6:O_2 ratio is used to modulate the F concentration with respect to the O concentration because in the range of SF_6-to-O_2 ratios used here, the ion current density remains

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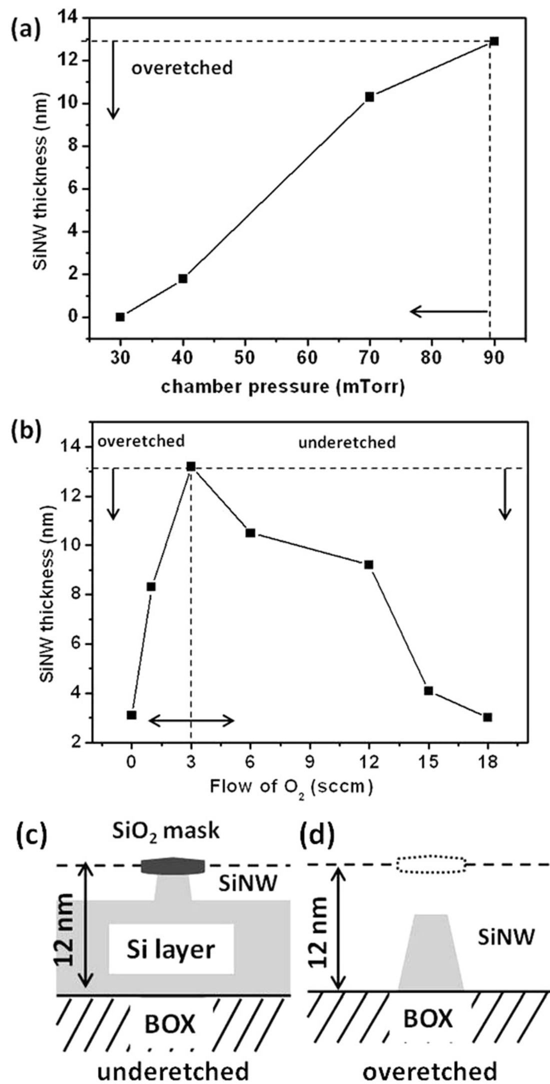

FIG. 2. (a) SiNW thickness as a function of the chamber pressure. (b) SiNW thickness as a function of the oxygen flow. (c) Scheme of the under-etched silicon structures. (d) Scheme of the over-etched silicon structures.

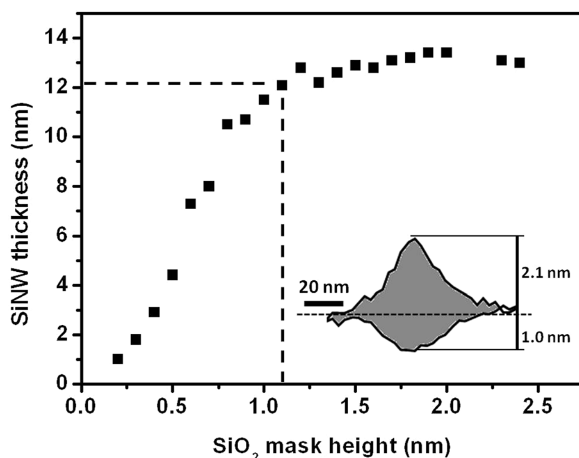

FIG. 3. Thickness of the silicon nanowires as a function of the height of the oxide masks (measured from the substrate baseline). The dotted line shows the value of the oxide height that generates a SiNW with a thickness identical to the active Si layer of the SOI. The inset shows the structure of the oxide mask fabricated by o-SPL. It shows that the oxide grows above and below the Si baseline.

practically constant. Consequently, the competition between F and O to react with Si can be described by the following reactions:

$$Si + xF + yO \rightarrow SiF_xO_y, \quad (1)$$

$$Si + 4F \rightarrow SiF_4 \ \text{(etching reaction)}, \quad (2)$$

$$Si + 2O \rightarrow SiO_2 \ \text{(passivation reaction)}. \quad (3)$$

The probability of F to react with SiO_2 is two orders of magnitude smaller than with Si, consequently, by changing the oxygen flow is the etching rate of Si what is affected.[32]

The width of the fabricated silicon nanowires is very close to the width of the oxide masks (Table I). Oxide masks with similar heights (1.1–1.4 nm) and widths (24–35 nm) give silicon nanowires of similar sizes with heights in the 12.7–13.5 nm range and widths in the 24–39 nm range. Those results indicate that the above etching parameters yield a directional and reproducible process.

Figure 3 shows the thickness of the SiNW as a function of the height of the o-SPL oxide with respect to the Si baseline. The etching conditions are 10 W of rf-power, 90 mTorr of chamber pressure, a gas mixture of SF_6:O_2 (12 sccm: 3 sccm), and an etch time of 126 s. The intersection point of Fig. 3 shows that an o-SPL mask of 1.1 nm in height enables the transfer of a 12 nm thick SiNW, this is, the thickness of the nanowire matches the thickness of the Si layer of the SOI. This means that the Si under the mask has not been removed during the process. It also implies that the whole oxide mask has been removed. By reducing the oxidation voltage from 21 V to 15 V, the oxide mask height changes from 1.1 nm to $\sim$0.3 nm. Those extremely thin masks in combination with the above RIE parameters enable the fabrication of SiNWs with thickness in the range of 2–12 nm. We note that the SPL oxide grows above and below the Si baseline. The inset shows the o-SPL mask before and after its etching in HF. Here, the oxide height is obtained by measuring the oxide that protrudes from the Si baseline. The o-SPL experiments give a height/depth oxide ratio of about 1.7–1.9. The oxide grown below the surface represents about 35% of the total thickness. Those values are very close to those reported on p-type Si(100).[33]

By using oxide masks with a thickness smaller than 1.1 nm and applying the above etching conditions, we can fabricate sub-12 nm SiNW down to 2 nm. This implies that SiNW of cross-sections below 100 nm^2 ($3 \times 30\,nm^2$) could be fabricated. Those values represent the smallest Si nanowire cross-section fabricated by any top-lithography.

The selectivity of the process is estimated from the angles of the mask and the transferred SiNW by using the expression[34,35]

$$S = \frac{\tan \theta_{nw}}{\tan \theta_{mask}}. \quad (4)$$

Figure 4 shows the cross-sections and AFM images of an o-SPL mask (Fig. 4(a)) and its corresponding SiNW (Fig. 4(b)) after applying the conditions determined here to preserve the initial thickness of the Si layer. By applying Eq. (4) to a series of masks and their resulting Si structures,

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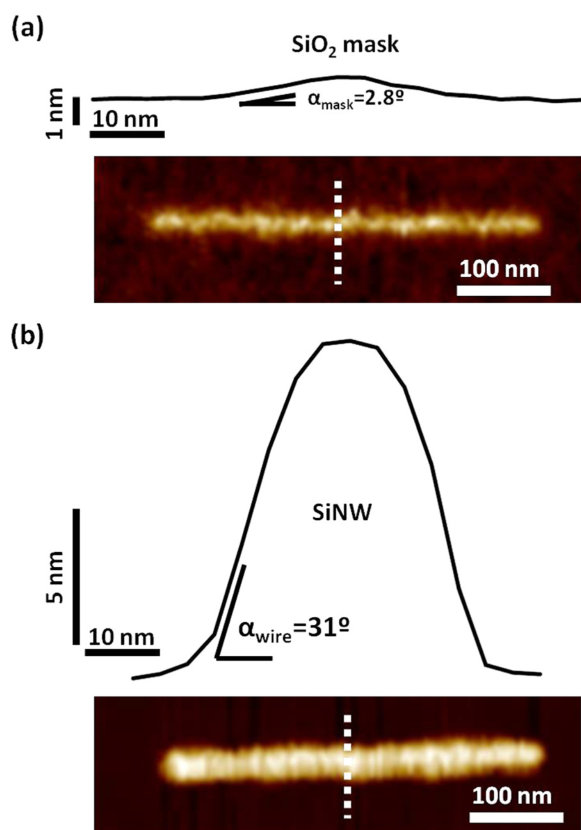

FIG. 4. (a) AFM image and cross-section of a 1.1 nm high oxide mask. (b) AFM image and cross-section of the silicon nanowire after the optimum etching process described in the text was applied to the mask shown in (a). Both cross-sections are at the same scale.

we obtain a selectivity average value of 11 for the above etching conditions.

We have determined the etching conditions to achieve a selectivity of about 11 between Si and silicon oxide. Under those conditions, the oxide masks and the patterned silicon nanowires have similar widths. Oxidation SPL enables the fabrication of extremely thin silicon oxide masks. By fabricating masks with heights below 1.1 nm, we can fabricate silicon nanowires with thicknesses below 12 nm. In particular, a mask of 0.4 nm generates a silicon nanowire of 3 nm in thickness. The channel of those nanowires is about 100 nm^2 which represents the smallest section of a single silicon nanowire fabricated by any top-down lithography.

This work was funded by the European Union FP7/2007-2013 under Grant Agreement No. 318804 (SNM).

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