Sub-20 nm patterning of thin layer WSe_2 by scanning probe lithography

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The electronic properties of thin layer transition metal dichalcogenides have raised considerable interest in the fabrication of advanced field-effect transistors and ultrasensitive sensors. Downscaling those devices to the nanoscale depends on the development of cost-effective and robust alternative nanolithographies. Here we demonstrate the direct, resist-less and reproducible nanopatterning of tungsten diselenide thin layers. By using oxidation scanning probe lithography we have generated arrays of dots with a width of 13 nm and periodicity of 40 nm. We have also patterned a point contact of 35 nm and a nanoscale field-effect transistor. The direct and resistless fabrication of WSe_2 nanoscale devices by oxidation scanning probe lithography (o-SPL) opens a straightforward and reliable method for processing transition metal dichalcogenides materials.

In the last years, thin layer transition metal dichalcogenides (TMD) have been used to fabricate novel electronic and optoelectronic devices. TMD materials have several attractive features such as their natural abundance, an adjustable band gap, the lack of dangling bonds on the surface and a high mechanical robustness and flexibility.[1,2] Their few-layer thickness enables a high electrostatic control, which make them suitable for developing a variety of ultrasensitive sensors.[3-5] In particular, WSe_2 is receiving a significant attention for designing optoelectronic devices because its intrinsic ambipolar transport.[6,7] Consequently, it is being used to fabricate a variety of prototypes such as photodetectors,[8,9] label-free biosensors[10] and CMOS logic circuits.[11] Despite their promising properties, TMD devices need to overcome several limitations to be considered as viable alternative for the fabrication of semiconductor devices.[12] One of these challenges is the availability of reliable and cost-effective lithographic methods with sub-50 nm patterning features.

Scanning probe lithography (SPL) is a serial nanolithography method which has demonstrated patterning and device fabrication capabilities at the sub-20 nm scale.[13] A variety of silicon nanowire devices and ionic conducting layers have been fabricated by oxidation SPL[14,15] while thermal-SPL has enabled the three-dimensional nanopatterning of a variety of objects.[16] SPL has been used to pattern conductive polymers,[17] layered materials such as graphene,[18,19] MoS_2,[20,21] and graphene oxide.[22,23] In fact, some exploratory patterning of a few micrometers thick WSe_2 was reported in the early days of atomic-scale modification of surfaces by probe microscopy.[24,25]

Here we report the direct chemical modification of selected regions of a few layers WSe_2 flake with sub-20 nm resolution by oxidation SPL. Dots, nanowires and nanoribbons have been fabricated. The patterns generated by o-SPL can be etched by immersion in water. This process transforms the nanopatterns into nanoscale dielectric barriers on the flake surface which could lead to the fabrication of quantum point-contacts and room-temperature WSe_2 nanoscale field-effect transistors (FETs).

The scheme of the o-SPL nanopatterning of WSe_2 is shown in Fig. 1(a). Freshly cut pieces of 270 nm thermal oxide SiO_2 on Si are prepared by applying a cleaning protocol of three sonication cycles in a dissolution of $NH_4OH:H_2O_2:H_2O$ (1:1:2) during 10 minutes each and a 5 minutes cycle of sonication in deionized water. The WSe_2 flake (HQ Graphene, Netherlands) is transferred onto the SiO_2 by first placing the WSe_2 flake on a Polydimethylsiloxane (PDMS) film (by mechanical contact) and then using the PDMS to paste it onto the silicon dioxide.[26] The flakes are chosen according to their thickness by combination of the colour contrast given by optical microscopy and AFM characterization.[27] The flake thickness ranges from 4 to 12 nm.

The oxidation SPL (o-SPL) experiments were performed by operating the atomic force microscope (dimension V, Bruker, USA) in the amplitude modulation mode with a free amplitude in the 5-10 nm range and a set point amplitude/free amplitude ratio of about 0.9.[28] The local anodic oxidation experiments were carried out by using n+-doped silicon cantilevers (NCH-W, NanoWorld, Germany) with a force constant of about 40 N/m and a resonant frequency of about 300 kHz. During the nanolithography process, the tip and the sample were kept in a closed chamber to control the relative humidity, in the range of 40% - 50% and the temperature at approximately 25°C. The tip is biased negatively with respect to the sample. The height and the width (FWHM) of the patterns are modulated by adjusting the amplitude and duration of the voltage pulse.

To fabricate WSe_2 nano-FETs we have used photolithography to pattern the source and drain electrodes at the opposite sides of the flake by electron beam evaporation of 20 nm of Ti followed by 80 nm of Au. After that, the sample is treated with oxygen plasma for 30 seconds to eliminate the resist residues. At this step, a micro-channel back-gated thin-layer WSe_2 FET is obtained. The silicon oxide and the bottom silicon act, respectively, as the gate dielectric and the back gate. Oxide barriers are fabricated by o-SPL to achieve FETs features in the nanoscale range. After etching of the oxide patterns by immersion in deionized water for 30 s, a nano-channel thin-layer WSe_2 FET is obtained. The device undergoes a rapid thermal annealing treatment (RTA) at 250 ºC for 1 h to improve the metal/flake contact and the overall electrical performance.

Fig. 1(b) shows an AFM topographic image of an array of dots fabricated by changing the voltage (from bottom to top) of 9, 10.5, 12, 13.5 and 15 V and the oxidation time (from left to right) of 0.3, 0.6, 0.9, 1.2 and 1.5 ms. The relative humidity and the free amplitude were, respectively, 50 % and 5 nm. The cross sections of the dots obtained at 0.9 ms for different voltages show features with heights ranging from 2 nm to 8 nm and FWHM from 31 nm to 40 nm (Fig. 1(c), top). The cross sections of the dots obtained by applying a 12 V pulse for different times show features with heights ranging from 3 nm to 8 nm and FWHM from 28 nm to 43 nm (Fig. 1(c), bottom). Fig. 1(d) shows an array of 50x50 dots with a periodicity of 40 nm. The dots have, respectively, a height and FWHM of 1 nm and 13 nm (average values). The dots have been fabricated with voltage, duration, relative humidity and free amplitude, respectively, of 29 V, 1.8 ms, 39% and 5 nm. Additional studies on the dependence of the dot size (height and width) on the voltage, time and relative humidity show that the size increases by increasing any of the above parameters (applied voltage, time and relative humidity). In the range of the experimental parameters used here, V=15-29 V, t=0.2-2 ms and RH=30-55 %), the dot size shows a near linear dependence with any of the above parameters.

The chemical nature of the generated patterns could be ascertained by observing that the process is polarity-dependent and that the patterns are soluble in water. The AFM topographic images of an array of lines, their cross sections and the grooves they leave after immersion in deionized H_2O for 30 s are shown, respectively, in Fig. 2(a) and 2(b). The presence of grooves indicates that the pattern also grows in the vertical direction below the surface baseline. The dependence of the patterning process on the bias polarity and the etching in water is compatible with the generation of WO_3.[29] The nanopatterns fabricated by o-SPL on other materials such as Si, Ti or GaAs have been explained based on an anodic oxidation process.[30] Based on those results, we propose that the nanostructures are oxides created by a field-induced electrochemical reaction occurring between the tip and the sample. We propose the following reaction [25]

$$WSe_2 + 9H_2O + 14h^+ \rightarrow WO_3 + 2SeO_3^{2-} + 18H^+ \quad (1)$$

The o-SPL oxide growth should occur above and below the WSe_2 baseline.[31] To estimate the total oxide thickness we have measured the dependence of the pattern depth (after etching) with the height (pre-etching) (Fig. 2(c)). The slope of the linear relationship shown in Fig. 2(c) indicates that about 54% of the oxide grows above the surface baseline.

Fig. 3(a) shows two opposing marks that confined a region of WSe_2 of 35 nm in width. By etching the above patterns in H_2O, the central region of 35 nm in width is preserved. This scheme could be used to fabricate quantum point-contact devices. Fig. 3(c) and 3(d) show the fabrication sequence of a nano-channel thin-layer WSe_2 FET by o-SPL. The width of the flake is about 1 μm in its narrowest spot. Two parallel oxide lines are patterned along the length of the flake to reduce the conduction area. Two lines perpendicular to the channel length are patterned to prevent the current leakage outside the conduction path (Fig. 3(c)). The oxidation parameters are set to generate an oxide that spans the whole flake thickness. This ensures the electric isolation of the nanoscale channel from the rest of the flake. From Fig. 3(c), the test patterns prior to the nano-channel fabrication can be seen on the left side of the flake. Fig. 3(d) shows the flake after the removal of the oxide lines by etching in deionized water for 30 s, leaving a final conduction channel with a width of 80 nm in its narrowest section.

WSe_2 FET devices show a variety of responses from devices which are predominantly n-channel FETs,[32,33] to predominantly *p*-channel FETs[34] or ambipolar.[10] The layer thickness controls the carrier type response from *p*-type layers with a thickness below 5-6 nm to ambipolar to *n*-type for thicker flakes. The FET devices fabricated here behave as predominantly *p*-channel transistors.

Fig. 4(a) shows the output curve of a nano-FET fabricated by o-SPL. The I-V measurements were performed at room temperature in a probe station (Everbeing EB 06, Taiwan) with a semiconductor analyzer (Keithley 4200). The measurements are performed inside a sealed and dark chamber to control the relative humidity level and isolate the device from the external light. The inset shows an optical image of the Ti/Au electrodes and the WSe_2 flake bridging them.

To illustrate how the channel width modifies the conduction of the device, we compare the transfer curves before and after patterning by o-SPL (Fig. 4(b)). The unpatterned (initial) FET device has a 1.3 μm wide channel (Fig. 4(b)). The curves have been acquired by using the same values of source-to-drain and gate voltages. Two major differences are observed in the transfer curves. The subthreshold swing (SS) of the nano-FET is significant better that the one of the unpatterned device (2.7 V/dec *versus* 8.2 V/dec). These values are still high for relevant electronics applications. The above SS values are controlled by the type of dielectric and gate configuration used here (back-gated). The on/off ratio has also improved after o-SPL. Overall, the above features demonstrate that the lithography steps involved in o-SPL do not deteriorate the electronic properties of the original flakes. The inset shows a section of the channel with a width of 240 nm.

Oxidation scanning probe lithography provides a direct and resistless approach to pattern tungsten diselenide surfaces with sub-20 nm features. The depth of the local oxides is controlled by the voltage and oxidation time. By etching the patterns in water we obtain dielectric barriers that could span the whole thickness of the WSe_2 flake. We have fabricated a few layer WSe_2 nanoscale transistors with relevant spatial features in the 80 to 250 nm range. Oxidation SPL provides an approach with a minimum of lithographic steps to fabricate a variety of nanoscale transition metal dichalcogenides devices.

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Figure captions

Figure 1. (a) Scheme of o-SPL to pattern a few layer WSe_2. (b) AFM topographic image of an array of dots fabricated under different conditions. The oxidation voltage is varied in the vertical axis from 9 V to 15 V (bottom to top). The oxidation time is varied in the horizontal axis from 0.3 ms to 1.5 ms (left to right). (c) Cross sections along the lines marked in (a). (d) Array of dots patterned by o-SPL on a few layer WSe_2 flake. The dots are 13 nm in width, 1 nm in height and are separated by 40 nm. o-SPL parameters, V_{ox}=29.1 V, t_{ox}=1.8 ms, RH=38.5 %. The inset shows a higher resolution image of the marked region.

Figure 2. (a) AFM topographic images of an array of lines before (top) and after a 30 s etching in H_2O (bottom). (b) The cross-sections along the lines marked in (a) show that teh etching in water removes the o-SPL patterns. This indicates that the patterns are made of a tungsten oxide. (c) Linear dependence of the depth of the trenches (after etching in H_2O) with the height of the o-SPL pattern (as measured from the flake baseline).

Figure 3. (a) 35 nm constriction fabricated on a few layer WSe_2 flake. o-SPL parameters, V_{ox}=18 V, t_{ox}=0.2 ms, RH=38%. (b) Etching in water removes the oxide and leaves a dielectric barrier separating the WSe_2 constriction from the main WSe_2 flake. (c) AFM topographic image of the oxides fabricated on the WSe_2 flake. After o-SPL patterning, the channel of the transistor is 80 nm wide. Patterning parameters are V_{ox}= 16.5 V, t_{ox}= 0.5 ms and a RH of 44%. Some test patterns to find the optimum o-SPL parameters are enclosed in a rectangle. (d) AFM topographic image of the region shown above after 30 s H_2O etching.

Figure 4. (a) Output curves of a WSe_2 nano-FET measured in ambient conditions. The inset shows an optical microscopy image of the Ti/Au electrodes and the flake bridging them. (b) Transfer curves of a FET before and after the channel has been reduced by o-SPL from 1.3 μm to 240 nm. The nano-FET shows an improvement of the transistor response (2.7 V/dec *versus* 8.2 V/dec). The high values of the SS are attributed to the type of dielectric (silicon dioxide) and the back-gate configuration of the FET. The inset shows an AFM image of the nano-FET channel.

References

[1] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, Nat. Nanotechnol., **9**, 768 (2014)

[2]A. Kuc, T. Heine, and A. Kis, MRS Bulletin, **40**, 577 (2015)

[3]N. Perea-López, A. L. Elías, A. Berkdemir, A. Castro-Beltran, H. R. Gutierrez, S. Feng, R. Lv, T. Hayashi, F. López-Urias, S. Ghosh, B. Muchharla, S. Talapatra, H. Terrones, and M. Terrones, Adv. Funct. Mater., **23**, 5511 (2013)

[4]D. Sarkar, W. Liu, X. Xie, A. C. Anselmo, S. Mitragotr, and K. Banerjee, ACS Nano, **8**, 3992 (2014)

[5]Y. Zhang, B. Zheng, C. Zhu, X. Zhang, C. Tan, H. Li, B. Chen, J. Yang, J. Chen, Y, Huang, L. Wang, and H. Zhang, Adv. Mater., **27**, 935 (2015)

[6]S. Das, and J. Appenzeller, Appl. Phys. Lett., **103**, 103501 (2013)

[7]A. Allain, and A. Kis, ACS Nano, **8**, 7180 (2014)

[8]W. Zhang, M.-H. Chin, C.-H. Chen, W. Chen, L.-J. Li, and A. T. S. Wee, ACS Nano, **8**, 8653 (2014)

[9]D. J. Groenendijk, M. Buscema, G. A. Steele, S. M. deVasconcellos, R. Bratschitsch, H. S. J. van der Zant, and A. Castellanos-Gomez, Nano Lett., **14**, 5846 (2014)

[10]H. Nam, B.-R. Oh, M. Chen, S. Wi, D. Li, K. Kurabayash, and X. Liang, J. Vac. Sci. Technol. B, 33, 06FG01-1 (2015)

[11]L. Yu, A. Zubair, E. J. G. Santos, X. Zhang, Y. Lin, Y. Zhang, and T. Palacios, Nano Lett., **15**, 4928 (2015)

[12]X. Duan, C. Wang, A. Pan, R. Yu, and X. Duan, Chem. Soc. Rev., **44**, 8859 (2015)

[13]R. Garcia, A. W. Knoll, and E. Riedo, Nat. Nanotechnol., **9**, 577 (2014)

[14]Y. K. Ryu, M. Chiesa, and R. Garcia, Nanotechnology, **24**, 315205 (2013)

[15]J. Berson, D. Burshtain, A. Zeira, A. Yoffe, R. Maoz, and J. Sagiv, Nat. Mater., **14**, 613 (2015)

[16]D. Pires, J. L. Hedrick, A. De Silva, J. Frommer, B. Gotsmann, H. Wolf, M. Despont, U. Duerig, and A.W. Knoll, Science, **328**, 732 (2010)

[17]H. Liu, S. Hoeppener, and U. S. Schubert, Adv. Func. Mat., **26**, 614 (2016)

[18]R. K. Puddy, C. J. Chua, and M. R. Buitelaar, Appl. Phys. Lett., **103**, 183117 (2013)

[19]N. Kurra, R. G. Reifenberger, and G. U. Kulkarni, ACS Appl. Mater. Interface, **6**, 6147 (2014)

[20]F. M. Espinosa, Y. K. Ryu, K. Marinov, D. Dumcenco, A. Kis, and R. Garcia, Appl. Phys. Lett., **106**, 103503 (2015)

[21]M. Donarelli, F. Perrozzi, F. Bisti, F. Paparella, V. Feyer, A. Ponzoni, M. Gonchigsuren, and L. Ottaviano, Nanoscale, **7**, 11453 (2015)

[22]Z. Wei, D. Wang, S. Kim, S.-Y. Kim, Y. Hu, M. K. Yakes, A. R. Laracuente, Z. Dai, S. R. Marder, C. Berger, W.P. King, W. A. de Heer, P. E. Sheehan, and E. Riedo, Science, **328**, 1373 (2010)

[23]M. Lorenzoni, A. Giugni, E. Di Fabrizio, F. Pérez-Murano, A. Mescola, and B. Torre, Nanotechnology, **26**, 285301 (2015)

[24]R. G. Garcia, Appl. Phys. Lett., **60**, 1960 (1992)

[25]M. Böhmisch, F. Burmeister, J. Boneberg, and P. Leiderer, Appl. Phys. Lett., **69**, 1882 (1996)

[26]A. Castellanos-Gomez, N. Agraït, and G. Rubio-Bollinger, Appl. Phys. Lett., **96**, 213116 (2010)

[27]M. M. Benameur, B. Radisavljevic, J. S. Héron, S. Sahoo, H. Berger, and A. Kis, Nanotechnology, **22**, 125706 (2011)

[28]M. Calleja, and R. Garcia, Appl. Phys. Lett., **76**, 3427 (2000)

[29]K. M. Andersson, and L. Bergström, Int. J. Refract. Met. H., **18**, 121 (2000)

[30] G. Mori, M. Lazzarino, D. Ercolani, L. Sorba, S. Heun, and A. Locatelli, J. Appl. Phys., **97**, 114324 (2005)

[31]Y. K. Ryu, P. A. Postigo, F. Garcia, and R. Garcia, Appl. Phys. Lett., **104**, 223112 (2014)

[32]J. Kang, W. Liu, D. Sarkar, D. Jena, and K. Banerjee, Phys. Rev. X, **4**, 031005 (2014)

[33]W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, Nano Lett., **13**, 1983 (2013)

[34]N. R. Pradhan, D. Rhodes, S. Memaran, J. M. Poumirol, D. Smirnov, S. Talapatra, S. Feng, N. Perea-López, A. L. Elias, M. Terrones, P. M. Ajayan, and L. Balicas, Sci. Rep., **5**, 8979 (2015)

Figures

Figure 1

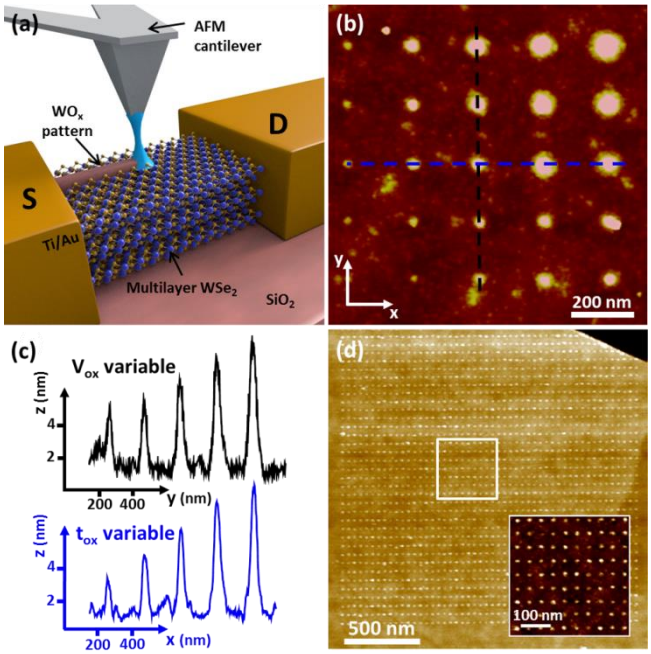


Figure 2

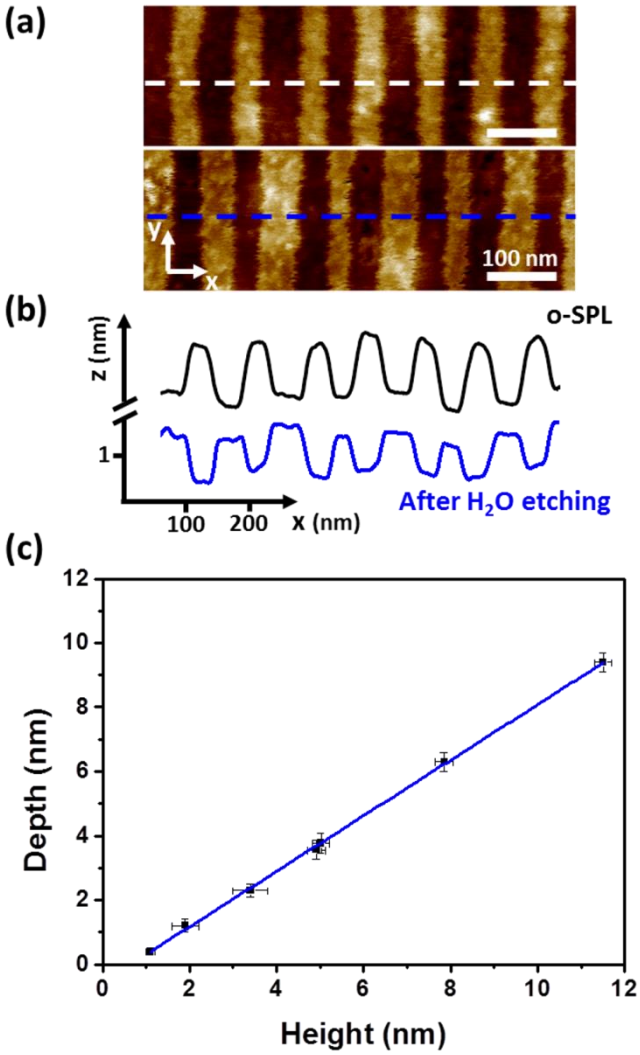

(a)
y
x
100 nm
(b)
o-SPL
z (nm)
1
After H_2O etching
100
200
x (nm)
(c)
Depth (nm)
Height (nm)
0
2
4
6
8
10
12

Figure 3

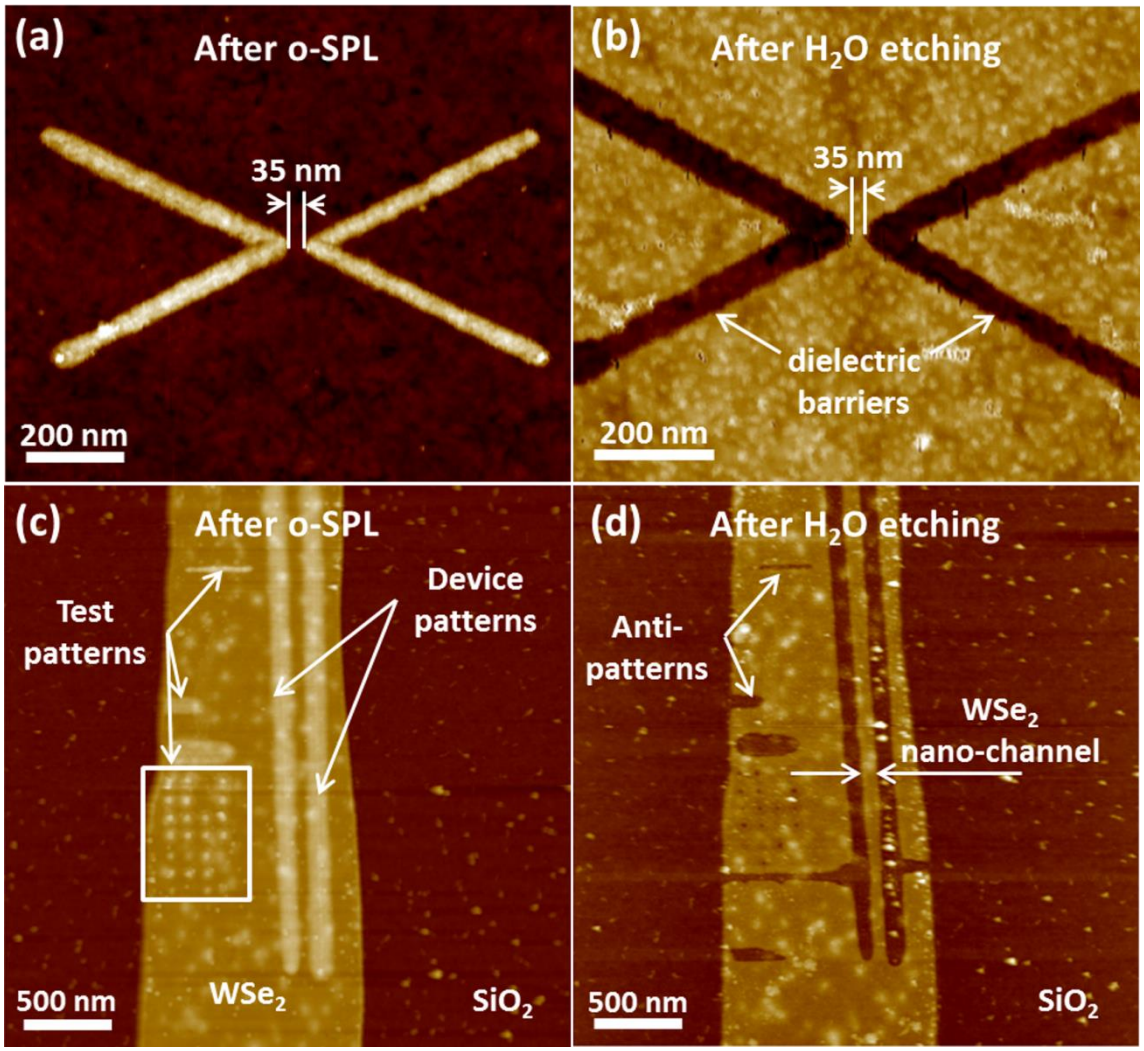
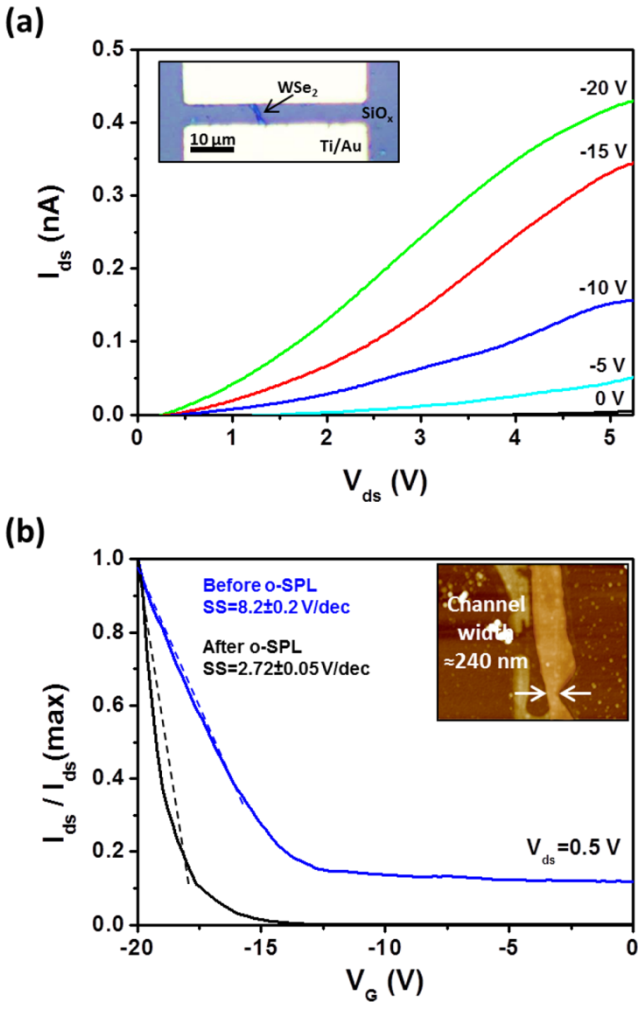

(a)
After o-SPL
35 nm
200 nm
(b)
After H_2O etching
35 nm
dielectric barriers
200 nm
(c)
After o-SPL
Test patterns
Device patterns
500 nm
WSe_2
SiO_2
(d)
After H_2O etching
Anti-patterns
WSe_2 nano-channel
500 nm
SiO_2

Figure 4


(a)
WSe2
SiOx
10 µm
Ti/Au
-20 V
-15 V
-10 V
-5 V
0 V
Ids (nA)
Vds (V)
(b)
Before o-SPL
SS=8.2±0.2 V/dec
After o-SPL
SS=2.72±0.05 V/dec
Channel width ≈240 nm
Vds=0.5 V
Ids / Ids(max)
VG (V)