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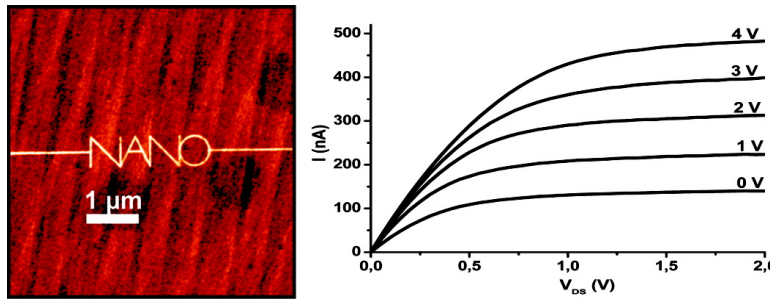

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Silicon Nanowire Transistors with a Channel Width of 4 nm Fabricated by Atomic Force Microscope Nanolithography

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ABSTRACT

The emergence of an ultrasensitive sensor technology based on silicon nanowires requires both the fabrication of nanoscale diameter wires and the integration with microelectronic processes. Here we demonstrate an atomic force microscopy lithography that enables the reproducible fabrication of complex single-crystalline silicon nanowire field-effect transistors with a high electrical performance. The nanowires have been carved from a silicon-on-insulator wafer by a combination of local oxidation processes with a force microscope and etching steps. We have fabricated and measured the electrical properties of a silicon nanowire transistor with a channel width of 4 nm. The flexibility of the nanofabrication process is illustrated by showing the electrical performance of two nanowire circuits with different geometries. The fabrication method is compatible with standard Si CMOS processing technologies and, therefore, can be used to develop a wide range of architectures and new microelectronic devices.

The development of ultrasensitive chemical, biological, and photovoltaic sensors has stimulated the interest on the fabrication and properties of silicon nanowires (SiNW) devices.[1−8] Reliable and high-performance silicon nanowire sensors are hard to fabricate due to the stringent characteristics they must have. First, as a ultrasensitive electrical sensors they must have a small diameter and a single-crystalline microstructure. Second, they must be properly interfaced with conducting microscopic contacts. Furthermore, the emergence of a SiNW-based technology will be benefited from a fabrication method compatible with integrated circuits technology (e.g., CMOS).

Thus several approaches are being pursued to fabricate semiconductor nanowires. Novel silicon nanowires were first fabricated by using multistep process based on a "bottom-up" vapor−liquid−solid technique[1] or metal-catalyzed chemical vapor deposition processes.[9] Several "down" approaches based on electron beam lithography,[10] reactive-ion etching,[11,12] or wet chemical etching process[13] have been applied to define SiNWs on silicon-on-insulator substrates. Similarly nanoimprint lithography[14] has been applied to fabricate arrays of silicon nanowires.

Atomic force microscope (AFM) nanolithography based on the spatial confinement of chemical reactions[15−17] has demonstrated a remarkable flexibility in the fabrication of 2 nm nanostructures with a 6 nm lateral spacing,[18] sophisticated superconducting single photon detectors,[19] masks for functional oxides,[20] novel etch-resistant resists,[21,22] templates for the growth molecular magnets,[23] or directed self-assembly.[24] The technique has also enabled the fabrication of submicrometer-size field-effect transistors.[25−28]

Here, we demonstrate that AFM nanolithography based on the local oxidation of a silicon-on-insulator surface enables the fabrication of SiNWs field-effect transistors with 4 nm channel widths. The transistors show good electrical characteristics. The presented nanolithography method has a high degree of flexibility and is compatible with many integrated circuit processes.

We have used an atomic force microscope to define a narrow silicon dioxide mask on top of a silicon-on-insulator substrate. The mask, a long and narrow stripe of silicon dioxide, is fabricated by applying voltage pulses between the AFM silicon probe and the silicon surface. The voltage pulse induces the formation of a water meniscus and the subsequent anodic oxidation of the surface. The next step involves the chemical etching of the unmasked silicon by either wet or dry processes. After etching, the local oxide mask is removed by HF and SiNWs are contacted to micrometer size platinum or gold source and drain contacts by electron beam lithography.. The main steps of the process are schematically presented in Figure 1.

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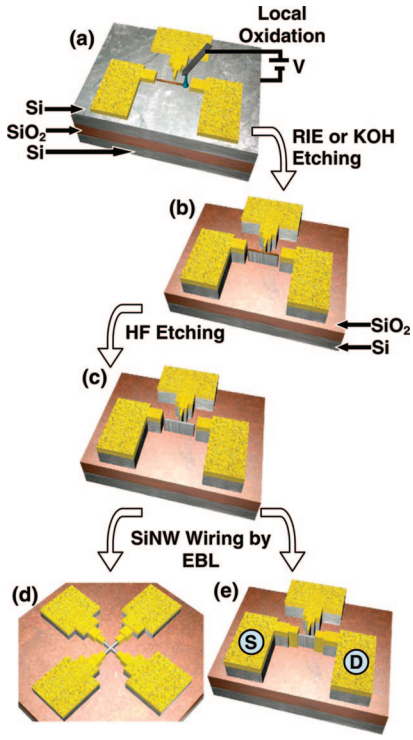

Figure 1. Scheme of the process to fabricate SiNWs circuits. (a) Schematics of the local oxidation process by using an AFM operated in the noncontact mode. The oxidation is mediated by the formation of a nanoscale water meniscus. Drain and source electrodes as well as the lateral marker were fabricated by electron beam lithography. (b) Dry or wet chemical etching of the unmasked silicon. (c) Removal of the local oxide mask by etching in HF. (d,e) Wiring of the different SiNW configurations (cross and line) to the electrode paths by e-beam lithography.

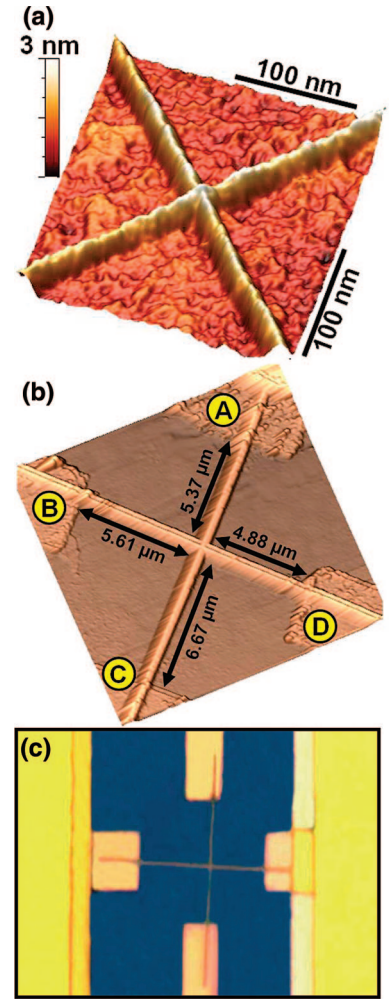

Figure 2. Images of a multiple-level SiNWs transistor. The device is formed by two perpendicular SiNW. (a) Amplitude modulation AFM image of the local oxide mask fabricated with the AFM. (b) Amplitude modulation AFM image of two perpendicular SiNWs (A−B and C−D) obtained after etching with KOH. (c) Optical image of the final device.

The first devices were performed on silicon-on-insulator (SOI) substrates with 150 nm thick device layer on top of a 100 nm buried oxide layer (both nominal values) purchased from University Wafer, MA, USA. The Si device layer has a resistivity ρ of 10−20 Ω cm. The surface nanolithography was done with a dynamic atomic force microscope operated in the low amplitude solution (noncontact) and with additional circuits to apply voltage pulses.[15] Noncontact AFM nanolithography was performed with doped n^+-type silicon cantilevers (Nanosensors, Germany). The force constant k and resonance frequency f_0 were about 35 N/m and 320 kHz, respectively. The cantilever was excited at its resonance frequency. To fabricate the silicon dioxide lines with the AFM, we apply a sequence of voltage pulses. The sample is biased positively with respect to the tip. Typical voltage pulses for the nanofabrication process are about 36 V and they last for 100 μs. A continuous line is obtained when the size of the individual dots is larger than the lateral distance between pulses. The wet etching was performed at 50 °C with a dilute solution (20%) of KOH in deionized water. The unmasked silicon layer was removed after 2 s. The electrical characterization of the device has been done with a HP4145B semiconductor parameter analyzer.

The present AFM nanolithography approach is rather flexible and enables us to fabricate complex circuits such as the four-arm transistor shown in Figure 2 or the transistor depicted in Figure 5a. The circuit showed in Figure 2 is formed by two perpendicular SiNWs (A−B and C−D), and the AFM images reveals the structure and size of the device. Figure 2a shows an image of the silicon oxides lines made by AFM at the crossing region. After the etching, Figure 2b, one can observe the silicon nanowires contacted to the electrodes. Finally, Figure 2c shows an optical image of the final circuit. The width enlargement of the nanowire in the base is due to KOH etching.

The output characteristics of the four-arm transistor are shown in Figure 3. The different SiNW transistors show a noticeable dependence on the gate voltage (Figure 3e). The gate electrode is situated in the back side of the wafer. The small differences observed between the different transistors are attributed to the differences in the corresponding SiNW width and length. The above results show that local oxidation nanolithography is compatible with multiple oxidation processes on the same location. Here the central node had two successive oxidations which in turn enables the fabrication of complex nanoscale devices.

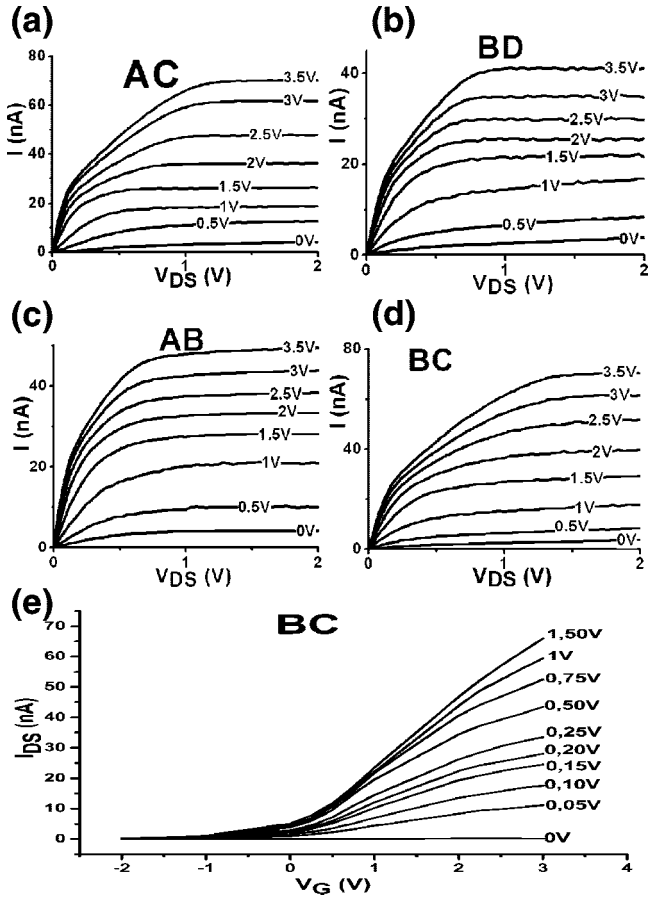

Figure 3. Current−voltage characteristics of a multiple-level SiNWs transistor device. (a−d) Current−voltage characteristics of the different nanowire paths (AC, BD, AB, BC). (e) Current-gate voltage characteristics for the BC path.

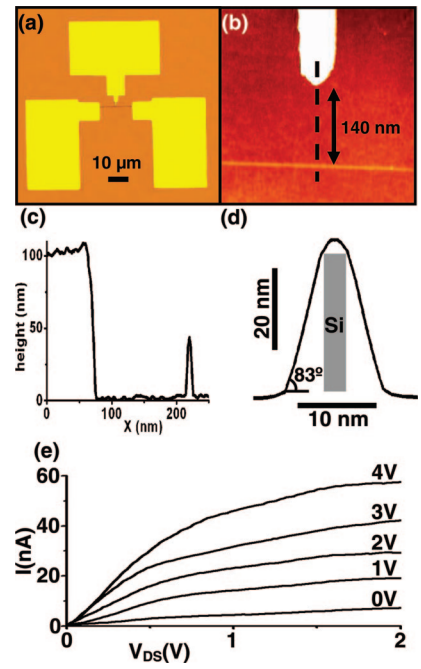

Figure 4. Images of a 4 nm channel width SiNWs transistor. (a). Optical image of a SiNW bridging two gold electrodes. A lateral gold marker is placed in the middle of the device. (b) Amplitude modulation AFM image of the lateral gate electrode and the nanowire. (c) AFM cross-section of the region marked in panel b. (d) Reconstruction of the SiNWs obtained from panel c. (e) Output characteristics of a 4 nm channel width Si nanowire field-effect transistor.

To reduce the dimensions of the nanowires, a new SOI wafer with a smaller silicon layer was needed. We used a SOI wafer with a 55 nm device layer (Si(100)) and a 61 nm buried oxide layer (IBIS Technology, MA, USA). Phosphorus was implanted to achieve $\rho = 0.01-0.02\ \Omega$ cm. In this case, the 55 nm silicon layer was etched by reactive ion etching (RIE). The RIE process produces vertical walls in the etching of the nanowires and this provide a drastic reduction of the nanowire volume with respect to the trapezoidal shape of the wires obtained by KOH etching. In addition RIE processes are compatible with Si CMOS technology. The silicon etching was made with a plama containing 80% SF_6 and 20% O_2 during 4 s in a Plasma RIE system (Oxford Instruments, U.K.)

Figure 4 shows a silicon nanowire transistor with a channel width of 4 nm. A single nanowire bridges the 14 μm gap between the drain and source gold electrodes. In this case we add, prior to the oxidation step, a side gold-marker to show that with this technique one can control the orientation of the SiNW (perpendicular to the side gold-marker) and the distance to the electrode. In our case the wire is separated by 140 nm from the gold marker (Figure 4b). The AFM cross-section shows the size of the wire with respect to the gold marker. The AFM image shows a nanowire with a trapezoidal cross-section with top and bottom apparent widths of 4 and 11 nm, respectively, and an apparent height of 37.5 nm. The top width is controlled by the AFM lithography. We have demonstrated that under the same conditions as described above the RIE produces structures with vertical sidewalls over 1000 nm (see image in Supporting Information). This leads us to conclude that the nanowire has a rectangular shape with a lateral size of 4 nm (Figure 4d). This conclusion is supported by the observation that the AFM image is always a convolution between the probe and the nanostructure. The ultrasharp silicon tips used to image the nanowire has an apex radius of ~2 nm and a half-cone angle of 8°. The apparent angle measured between the nanowire sidewalls, and its base is 83°. This value is close to the angle formed between the sidewall of the supersharp tip and the substrate baseline ~82°. This coincidence proves that the AFM image is the result of the convolution of a conical tip of half angle 8° and the nanowire.

The section of the above SiNW is equivalent to the section of a cylindrical wire of 6.6 nm in radius. The height of the silicon nanowire ≈35 nm was mainly controlled by the thickness of the device layer (~55 nm) and the RIE exposure time. We remark that on top of the nanowire there is a local oxide layer of about 2.5 nm. The output characteristics of the 4 nm channel width nanowire are shown in Figure 4e. The field-effect transistor has the gate electrode situated in the back side of the wafer.

The geometry of the nanowire depicted in Figure 5a illustrates the flexibility of the local oxidation nanolithography to fabricate small silicon nanowires of arbitrary geometry. The nanowire has a section with the shape of the term "NANO", that is, it includes linear and circular

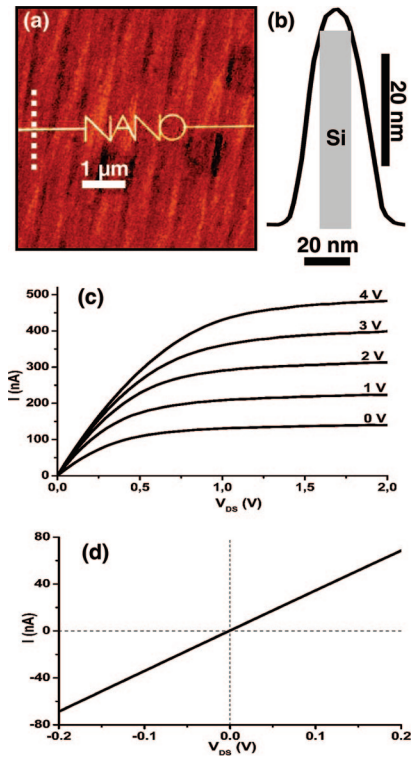

Figure 5. (a) AFM image (top view) of a SiNW that combines linear and circular regions. (b) Cross-section of the region marked in panel a. (c) Output characteristics of the 14 nm channel Si nanowire field-effect transistor. At both ends of the SiNW is contacted to platinum electrodes. (d). Resistance of the nanowire in the linear regime.

elements. In particular, the circle has a diameter of 550 nm. To make the process compatible with CMOS, the SiNW was etched by RIE and contacted to micrometer size platinum electrodes (90 nm of Pt on top of 10 nm of Ti). The reconstructed AFM cross-section shows a SiNW of about 14 nm in width and 36 nm in height (Figure 5b). The output characteristics are shown in Figure 5c. The total resistance of the device $R_t = 3$ MΩ can be obtained from the slope of the output curves in the linear regime (Figure 5d). The total resistance includes the contact resistance between the nanowire and the platinum electrodes (R_{Ci}), the resistance of the external circuit (R_{ext}) and the nanowire resistance (R_{NW})

$$R_t = R_{C1} + R_{C2} + R_{NW} + R_{ext} \quad (1)$$

An initial estimation of R_{NW} could be obtained from the bulk resistivity of the SOI wafer ($\rho = 0.01-0.02$ Ω cm) and the size of the nanowire. By applying Ohms' law

$$R_{NW} = \rho \frac{L}{A} \quad (2)$$

we obtain a value in the 2.8 MΩ range ($L = 7.22$ μm as the shortest path between source and drain contacts and $A = 504$ nm^2). Thus we find a good agreement between theoretical (Ohms' law) and experimental value The above agreement has a 2-fold value. First, it indicates that the contact resistance and external resistances are negligible with respect to R_{NW}, which in turns, implies that the electrical response is controlled by the nanowire. Second, the nanofabrication process does not alter the properties of the nanowire.

In conclusion, we have fabricated silicon nanowires with a channel width of 4 nm connected to microscopic conducting electrodes. We show that electrical properties of the fabricated field-effect transistors are dominated by the nanowire properties. We also show that the force microscope-based nanolithography used here is flexible and compatible with many standard processing technologies. To prove this, we have fabricated integrated circuits made of nanowires with linear and circular geometries.

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Supporting Information Available: This material is available free of charge via the Internet at http://pubs.acs.org.

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