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Electrical characteristics of silicon nanowire transistors fabricated by scanning probe and electron beam lithographies

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Abstract
Silicon nanowire (SiNW) field-effect transistors have been fabricated by oxidation scanning probes and electron beam lithographies. The analysis and comparison of the electron mobility and subthreshold swing shows that the device performance is not affected by the top-down fabrication method. The two methods produce silicon nanowire transistors with similar electrical features, although oxidation scanning probe lithography generates nanowires with smaller channel widths. The values of the electron mobility and the subthreshold swing, 200 $cm^2\ V^{-1}\ s^{-1}$ and 500 mV dec^{-1}, respectively, are similar to those obtained from bottom-up methods. The compatibility of top-down methods with CMOS (complementary metal–oxide–semiconductor) procedures, the good electrical properties of the nanowire devices and the potential for making sub-10 nanowires, in particular by using oxidation scanning probe lithography, make those methods attractive for device fabrication.

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon nanowires with high surface-to-volume ratio are the building blocks of highly sensitive devices such as label-free biosensors [1–6], chemical sensors [7, 8], electromechanical resonators [9, 10] and photovoltaic devices [11, 12]. Silicon nanowires have also been applied to interface natural neuronal networks [13, 14]. Bottom-up and top-down approaches are currently used to fabricate silicon nanowire (SiNW) field-effect transistors. Bottom-up methods are based on catalyst-assisted growth [15]. Those methods are able to generate nanowires with diameters smaller than 5 nm. Top-down approaches are based on the use of lithographic methods such as electron beam lithography [16], and nanoimprint [17] and scanning probe lithography [18, 19]. In the context of nanowire transistors, Schottky barrier nanowire FETs are attractive because they avoid the use of dopants and parasitic resistances [20–23].

The high spatial resolution of the atomic force microscope (AFM) and its positioning capabilities make it possible to fabricate a silicon nanowire in a predefined region of a circuit. Scanning probe lithography (SPL) based on an oxidation process provides a precise control over the shape of the nanowire on a flat surface; thus, straight or curved nanowires have been fabricated [18]. Similarly, the beam positioning in an electron microscope allows contacting the nanowire to the external macroscopic electrodes. Thus both SPL and electron beam lithography are currently being developed to fabricate SiNW transistors. Furthermore, top-down lithographies are compatible with complementary metal–oxide–semiconductor (CMOS) technology which makes them convenient for integrating SiNW transistors with other devices. However, there are no comparisons of the advantages or disadvantages among the different top-down lithographies in terms of the SiNW electrical properties. Such observations, to a certain

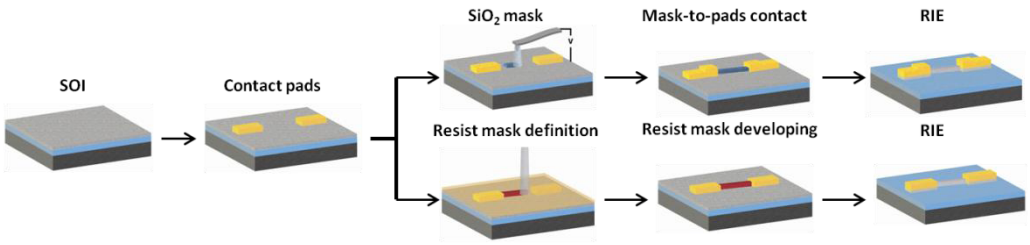

Figure 1. Scheme of the main SiNW fabrication steps in oxidation scanning probe lithography and electron beam lithography.

extent, also apply to other methods used to fabricate silicon nanowire devices.

Here, we apply two top-down nanolithographies [24–26]—oxidation scanning probe lithography (oSPL) and electron beam lithography (EBL)—to fabricate SiNW field-effect transistors. The two methods use as substrates chips cut from the same silicon-on-insulator wafer (SOI), which facilitates the direct comparison of the performance of the devices. In this study we measure the output and transfer characteristics of the SiNW FETs. From those curves, the electron mobility and subthreshold voltage can be deduced. Oxidation SPL and EBL have different fabrication steps; however, the electrical response of the transistors does not seem to be affected by the specific top-down fabrication method. The key factors that control the SiNW transistor properties are the size of the transistor channel and the electrical properties of the metal–nanowire contact at their interface. In this respect SPL and EBL produce channels of different sections, trapezoidal-like in oSPL and rectangular in EBL. In this study we have fabricated SiNWs with the full width at half-maximum (FWHM) being, respectively, 80 and 120 nm for SPL and EBL. The electron mobility and subthreshold swing are, respectively, 208 $cm^2\ V^{-1}\ s^{-1}$ and 499 mV dec^{-1} (SPL) and 200 $cm^2\ V^{-1}\ s^{-1}$ and 537 mV dec^{-1} (EBL). The electrical response of the devices improves significantly upon subjecting them to rapid thermal processing.

2. Nanofabrication methods

Figure 1 shows a scheme of the fabrication process for oSPL and EBL. The lithographies share several common elements: the SOI substrate, similar source and drain metal contacts and the removal of the unmasked regions of the top silicon layer by a reactive ion etching (RIE) system (PlasmaLab 80, Oxford Instruments, UK) with a plasma containing 20% O_2 and 80% SF_6 with 8–12 s pulses. Furthermore, a key element of oSPL and EBL for fabricating SiNWs is the generation of a narrow mask for etching. The chemical nature of the mask depends on the lithography: a narrow silicon dioxide stripe in oSPL and a negative cross-linked resist stripe for EBL.

The SOI substrates have a 57 nm thick Si top layer with a nominal resistivity of $\rho = 10$–$20\ \Omega$ cm and a 151 nm thick buried oxide layer (SIMOX (separation by implantation of oxygen), IBIS Technology, Danvers, MA). The SOI was cleaned by sonication using a protocol of three cycles in NH_4OH:H_2O_2:H_2O (1:1:2) for 12 min each and a last cycle of 5 min in deionized water. A fresh NH_4OH:H_2O_2:H_2O bath was used in each cycle. Then a photolithography step was performed to obtain the metal electrodes consisting of 5 nm of Cr and 40 nm of Au. Oxidation SPL is performed with a force microscope operated in the amplitude modulation mode [27, 28]. The AFM (Dimension V, Veeco, USA) was placed into a closed chamber to control the relative humidity. The oxidation was performed at a relative humidity of 60%. We have used n^+-type doped silicon cantilevers (model NCHV, Bruker) with a force constant of about 42 N m^{-1} and a resonant frequency of 320 kHz. The cantilever was excited at its resonant frequency. Typical values of the parameters used to write the oxide lines are applied pulses of 15–30 V with ms duration. Following this step, the SiO_2 masks are contacted with the marker electrodes via another photolithography step. The above protocol yields silicon dioxide masks of 2–4 nm in thickness.

In electron beam lithography, the etch masks were obtained by writing lines over a layer of negative resist (AR-N 7500.08, Allresist GmbH, Strausberg, Germany) which was previously spin-coated and cured on the silicon top layer of the SOI, and developing them in the corresponding developer (AR 300-47, Allresist) to remove the unexposed areas of the resist.

The last lithography step for both oSPL and EBL is the etching of the unmasked silicon by RIE. Figure 2 shows force microscopy images of a SiNW FET fabricated by oSPL (figure 2(a)) and EBL (figure 2(b)). For the two devices the electrical configuration is similar: a back-gated Schottky barrier field-effect transistor where the bridging nanowire between the source and drain electrodes acts as the transistor channel, the buried SiO_2 layer acting as the gate dielectric and the silicon substrate acting as a back gate.

The fabricated SiNWs were 5–10 μm in length and 30–50 nm in thickness. The nanowire width depends on the lithography method; typical values of FWHM are 60–80 nm in SPL and 100–150 nm in EBL. The height of the fabricated nanowires is mostly determined by the original thickness of the silicon layer of the SOI although it may be reduced by the etching process. The fabricated SiNWs differ in shape. The nanowire cross-section is close to rectangular in EBL, while it is more trapezoidal-like in SPL, as a consequence of the mask shapes (figure 2(c)). In the case of oxidation SPL, the trapezoidal shape of the SiO_2 features is transferred to the silicon nanowire during the etching process, while the EBL method leads to more rectangular wires with quite steep walls. To make the comparison we have chosen SiNWs of

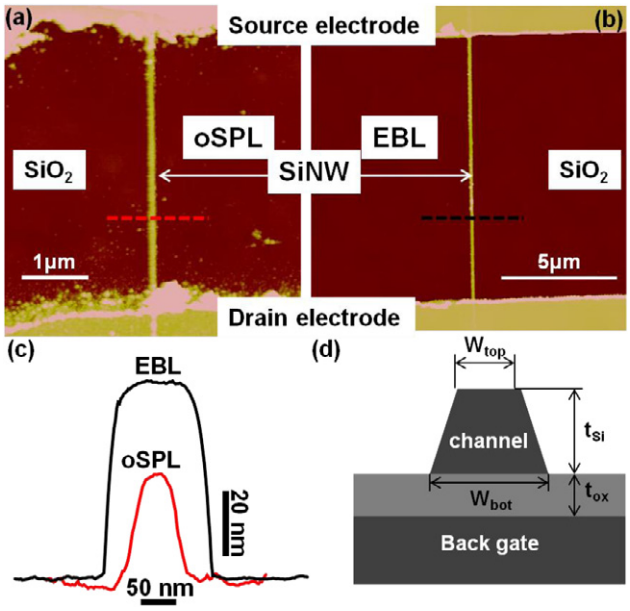

Figure 2. AFM images of two silicon nanowires. (a) Fabricated by oSPL. (b) Fabricated by EBL. (c) Cross-sections of the SiNWs marked in (a) and (b). (d) Cross-section scheme of a SiNW transistor.

comparable widths that correspond to nanowires of 80 nm (FWHM) for oSPL and 120 nm (FWHM) for EBL. However, the observed trends remain valid for the 11 SiNW FETs analyzed in this study.

The electrical properties of the devices have been measured as fabricated and after applying an annealing process consisting of a pulse of 300 °C for 30 s in a N_2 atmosphere. The process was performed with a rapid thermal processing oven (Rapid Thermal Processor AS-Micro, Annealsys, France).

3. Electrical properties of the SiNW transistors

The common parameters for characterizing the electrical performance of a SiNW transistor are the threshold voltage (V_{th}), the subthreshold swing (SS), the on/off current ratio and the electron mobility. The first three parameters can be extracted directly from the transfer curves. The electron mobility is given by the following expression [29]:

$$\mu_e = \frac{L^2 G_m}{C_{nw} V_{ds}} \tag{1}$$

where L, G_m, C_{nw} and V_{ds} are, respectively, the channel length, the transconductance, the nanowire–oxide–back gate capacitance and the drain–source voltage, respectively. The transconductance, $G_m = dI_{ds}/dV_g$ is calculated as the fit of the slope of the transfer curve above the threshold voltage. The capacitance of the nanowire–dielectric–gate interface requires taking into account the device geometry. To estimate the capacitance we have considered two different analytical models and finite-element simulations for different geometries of the nanowire–oxide–gate interface [30–32].

Let us start first with the expression for the parallel-plate capacitor model:

$$C_{nw}^{p} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} WL \tag{2}$$

where W and t_{ox} are, respectively, the width of the SiNW channel and the thickness of the dielectric (figure 2(d)).

Let us now consider the capacitance of a cylindrical nanowire surrounded by a dielectric:

$$C_{nw}^{c} = \frac{2\pi \varepsilon_0 \varepsilon_{ox}}{\cosh^{-1}(t/R)} L \tag{3}$$

where t is the distance from the center of the wire to the bottom gate electrode ($t = R + t_{ox}$).

Figure 3 shows finite-element simulations (COMSOL Multiphysics) of the electric field lines for the two models described above and for a trapezoidal SiNW. The latter geometry is very close to that of the fabricated nanowires. The field lines of the cylindrical model are a better approximation to those of the trapezoidal SiNW than those of the parallel-plate model. Thus the cylindrical model is expected to give a better estimation of the capacitance than the planar model. This is verified by calculating the capacitance of a nanowire with a length and height respectively of 10.5 μm and 32 nm. The value of the width is 85 and 20 nm for bottom and top sides (red section in figure 2(c)). For the parallel model the bottom side of the wire is taken. For the cylindrical model, the equivalent radius of the trapezoidal nanowire is obtained by matching the area of its section with that of a circle. For the above values we obtain for the parallel, cylindrical and trapezoidal cases, respectively, 0.2, 0.85 and 0.69 fF. Thus, the values of the capacitance of the fabricated SiNWs fall between the boundaries defined by the parallel-plate and cylindrical models, and, as expected, the cylindrical model gives a better estimation. The cylindrical model introduces a slight overestimation of the real value because it considers that a uniform dielectric surrounds the SiNW. However, in the fabricated nanowires a dielectric oxide isolates them from the gate electrode, but the top and lateral faces of the nanowire are surrounded by air which has a lower relative dielectric constant than the oxide ($\varepsilon_{air} = 1$ compared to $\varepsilon_{ox} = 3.9$) [31].

Once the capacitance has been estimated, the threshold voltage, the subthreshold swing and the electron mobility can be obtained from the transfer curves. The electrical characterization of the fabricated SiNW FETs was performed at room temperature with a setup consisting of a semiconductor characterization system (Keithley 4200) and a probe station (Everbeing EB 06, Taiwan).

Figure 4 shows the transfer curves of two typical nanowire FETs fabricated, respectively, by oSPL and EBL. The mobility and the subthreshold swing are, respectively, 102 $cm^2\ V^{-1}\ s^{-1}$ and 1172 mV dec^{-1} for the oSPL device, and 122 $cm^2\ V^{-1}\ s^{-1}$ and 1031 mV dec^{-1} for the EBL device. Those values are considerably poorer than the ones reported for transistors fabricated by bottom-up and by top-down approaches (table 2). The fabrication of nanowire transistors by electron beam and scanning probe lithographies involves

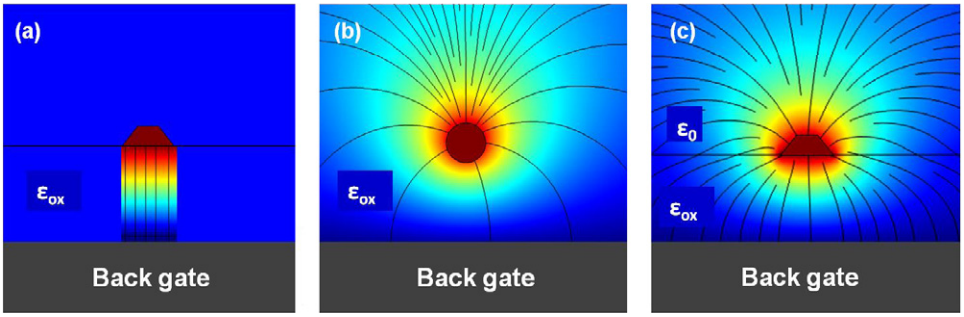

Figure 3. Finite-element simulation of the field lines for different models of the nanowire–dielectric–gate interface. (a) Potential drop and electric field lines for a parallel-plate capacitor. (b) Potential drop and electric field lines for a cylindrical model. (c) Potential drop and electric field lines for a trapezoidal Si nanowire on top of a SiO_2 dielectric. The potential drop is illustrated by the color changes.

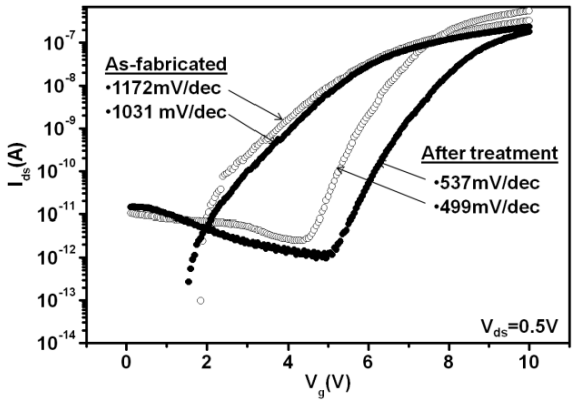

Figure 4. Transfer curves of the oSPL-fabricated (open circles) and EBL-fabricated (filled circles) SiNW transistors before and after applying a thermal pulse of 300 °C for 30 s in N_2. After the thermal treatment the subthreshold swings of the two transistors are considerably steeper.

Table 1. Electron mobility and SS values of SiNW transistors.

oSPL	EBL
As-fabricated properties	*As-fabricated properties*
μ_e ($cm^2\ V^{-1}\ s^{-1}$)	μ_e ($cm^2\ V^{-1}\ s^{-1}$)
82[a]	101[a]
217[b]	249[b]
102[c]	122[c]
SS ($mV\ dec^{-1}$)	SS ($mV\ dec^{-1}$)
1172	1031
After treatment properties	*After treatment properties*
μ_e ($cm^2\ V^{-1}\ s^{-1}$)	μ_e ($cm^2\ V^{-1}\ s^{-1}$)
167[a]	179[a]
444[b]	413[b]
208[c]	200[c]
SS ($mV\ dec^{-1}$)	SS ($mV\ dec^{-1}$)
499	537

[a] Cylindric wire on plane model.
[b] Parallel-plate model.
[c] Trapezoidal model.

several steps of processing, which may adversely affect the electrical properties of the as-fabricated SiNW devices. For example, the irregularities at the metal–semiconductor contacts could create defects that, in turn, could produce a poor and unstable electrical response of the devices [33]. However, the anomalous behavior that is usually observed in as-fabricated devices can be significantly reduced or removed by annealing the devices. For this reason, we annealed the devices by applying thermal pulses of 300 °C with duration of 30 s under an N_2 atmosphere.

Before annealing, the devices fabricated by EBL show a slightly better performance—higher mobilities and lower SS—than the ones fabricated by oSPL. This is probably related to the fact that the process of fabrication by EBL involves one step less than that by oSPL. This might favor the fabrication of devices with fewer interfacial states and impurities. The properties of all the devices show a significant improvement after the thermal annealing. We also observe that the values of the mobility of the oSPL and EBL devices become very similar, with a relative difference of 4%. From this we conclude that the electrical properties are independent of the fabrication method. The remaining differences could be explained in terms of the differences in size and geometry.

Figures 5(a) and (c) show the output characteristics of the two nanowire FETs shown in figure 4 after the thermal treatment. The curves show the linear as well as the saturation regimes and significant amplification behavior. Both devices are n-channel enhancement mode transistors, i.e., the transistors are off a zero gate voltage. The transfer characteristics in the linear region ($V_{ds} = 0.5$ V) of the transistors on both linear and logarithmic scales are plotted in figures 5(b) and (d). The curves are very similar, with independence of the fabrication method. The threshold voltage for the oSPL transistor is 7 V while for the EBL transistor it is 8 V. The on/off ratio is about 10^5 in both cases. The electron mobilities, calculated according to equation (1) with C_{nw} estimated using the trapezoidal model, are 208 $cm^2\ V^{-1}\ s^{-1}$ for oSPL and 200 $cm^2\ V^{-1}\ s^{-1}$ for EBL. The small numerical differences are attributed to the different geometries of the fabricated SiNWs.

Table 1 presents the values of the mobility of the nanowire transistors calculated according to the different capacitor models presented in this work. The spread of values underlines the importance of considering the real geometry to estimate the device parameters. Those values are in agreement with what has been reported from other bottom-up and

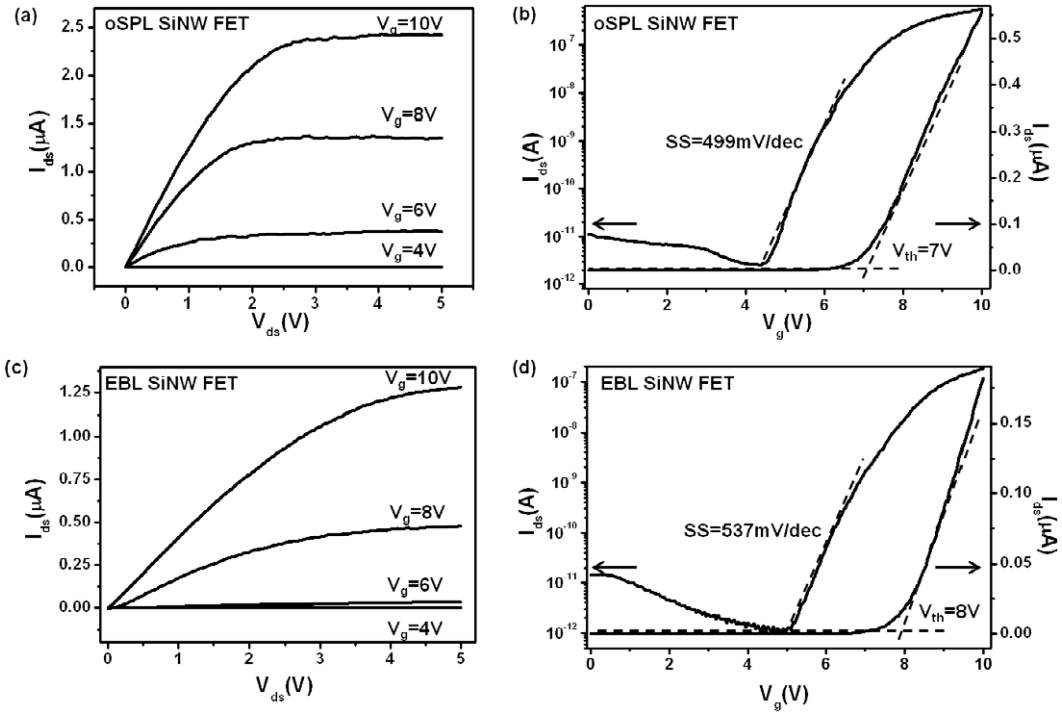

Figure 5. Output and transfer curves of SiNW transistors. (a) Output curves of a device fabricated by oSPL. (b) Transfer curves of the device characterized in (a). (c) Output curves of a device fabricated by EBL. (d) Transfer curves of the device characterized in (c).

Table 2. SiNW features from different fabrication methods.

Author [reference]	Fabrication method	Gate dielectric	Channel width (nm)	μ_e ($cm^2\ V^{-1}\ s^{-1}$)	SS ($mV\ dec^{-1}$)
Zheng *et al* [39]	Laser-assisted catalytic growth	60 nm ZnO_2	20	270	300
Allen *et al* [40]	VLS growth + channel etching	200 nm Si_3N_4	50	175	600
Chen *et al* [41]	Thermal oxidation	13.6 nm SiO_2	48	540	60
Huang *et al* [9]	Superlattice nanowire pattern transfer	4 nm SiO_2 + 6 nm HfO_2	10	268	168
This work	oSPL	151 nm SiO_2	80	208	499
	EBL		120	200	537

top-down fabrication approaches (table 2). The subthreshold swing values obtained from the transfer curves are 499 and 537 mV dec^{-1} for oSPL and EBL, respectively (figure 5). Those values are about one order of magnitude higher than the ideal values for FETs at room temperature (60 mV dec^{-1}). A theoretical calculation of the subthreshold swing SS is given by the expression [29]

$$SS = \ln 10 \left(\frac{kT}{q}\right)\left(1 + \frac{C_D}{C'_{nw}} + \frac{C_{it}}{C'_{nw}}\right) \quad (4)$$

where C_D is the depletion layer capacitance, C_{it} is the capacitance associated with the interface trap density and C'_{nw} is the gate/channel capacitance in the subthreshold regime [29]. Using as a first approximation the parallel-plate model capacitance for C_D and C_{nw}, equation (4) reduces to $SS \approx 60\ mV\ dec^{-1}\ (1+3t_{ox}/t_{Si}+C_{it}/C_{nw})$ [34]. Considering that in these devices $t_{ox} = 151$ nm and approximating t_{Si} as the height of the wire ≈50 nm (full depletion), we would obtain, in the ideal case of zero interfacial traps, a value of about 600 mV dec^{-1}, which is slightly higher than the values measured (∼500 mV dec^{-1}) after the thermal treatment. However, the above approximation does not fully apply to these devices, because of geometrical considerations. First of all, C_D is overestimated since the depletion length is comparable with the Debye length, which is of the order of 100 nm for the substrates used here. On the other hand, the value of C'_{nw} should take into account both the real geometry (trapezoidal) and the fact that, in the subthreshold regime, the nanowire–dielectric–back gate capacitance has an additional series term related to the depletion of the silicon gate electrode. Indeed, because of the relatively low doping, such a depletion length is comparable with the oxide thickness. As a consequence, the role of interfacial traps in affecting the subthreshold swing cannot be neglected, even after the thermal treatment. However, the observed decrease of the subthreshold swing indicates a reduction of the density of interfacial trap states. Furthermore, equation (4) indicates that the subthreshold swing would improve upon increase of C_{nw}, i.e. a reduction of the thickness of the dielectric. This is achieved by using alternative configurations like top gate [9, 35, 36], dual gate [37] and all-around gate [38]. However, those configurations impose a strong limitation

on using the nanowire transistors as sensors. Indeed, the state-of-the-art sensors based on SiNW FETs [1, 7, 20] have values of subthreshold swing comparable with the ones presented in this work.

4. Conclusion

Oxidation scanning probe and electron beam lithographies have been applied to fabricate silicon nanowire field-effect transistors using the same wafer platform. This enables a direct comparison of the above top-down lithographies with respect to the nanowire fabrication process. Under similar conditions, scanning probe lithography provides nanowires of smaller channel widths than electron lithography. We have measured the electron mobility and the subthreshold swing of the nanowire transistors. The measured values are, respectively, about 200 cm^2 V^{-1} s^{-1} and about 500 mV dec^{-1}. The two lithographies provide similar values. Furthermore, the parameters of the nanowires fabricated by top-down approaches are similar to those obtained by bottom-up lithographies. We remark that the subthreshold swing of the fabricated device is very close to its theoretical value. Here the values of the subthreshold swing were dominated by the thickness of the silicon dioxide dielectric layer. The agreement obtained validates the use of top-down lithographies for silicon nanowire fabrication. However, the as-fabricated devices show far from ideal transistor characteristics. Those features are easily removed by subjecting the nanowires to a thermal process.

Acknowledgments

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